IN THE SPECIFICATION

Please insert the following Summary after the paragraph beginning on page 1, line 19 of the application as filed.

SUMMARY

According to an example embodiment, a method of operating a network processor includes writing, to a shared memory accessible by multiple packet processing engines, a dynamic packet rule set, each rule specifying a packet offset, a data pattern, and an action code. The method further includes writing, to an instruction store for the packet processing engines, execution instructions referencing the dynamic packet rule set. The method further includes, on at least one of the packet processing engines, while processing a packet and in response to the execution instructions, loading a first packet rule from the dynamic packet rule set, comparing packet data at the packet offset specified in the first packet rule to the data pattern specified in the first packet rule, and, when the comparison indicates a match, performing an action indicated by the action code specified in the first packet rule.

According to another example embodiment, an integrated circuit includes a local memory capable of storing a rule table, the rule table organized with entries comprising a packet offset, a data pattern, and an action. The integrated circuit further includes a packet data queue to receive packet data, a rule fetch unit to fetch rules from the rule table, and a packet data fetch unit to fetch a segment of packet data from the packet data queue, based on the packet offset fetched by the rule fetch unit. The integrated circuit further includes match circuitry to compare the packet data segment fetched by the packet data fetch unit with the data pattern fetched by the rule fetch unit and an action unit to perform the action fetched by the rule fetch unit when the match circuitry indicates a match between the compared packet data segment and data pattern.

According to another example embodiment, a method of gathering statistics on packets received by a network processor, includes configuring a core processor to dynamically accept packet rule requests and place corresponding packet rules in a packet rule set area at a first memory region in an addressable memory space, at least one rule in the packet rule set specifying a packet offset, a data pattern, and a counter offset. The method further includes configuring a set of packet processing engines to sequence through the packet rule set, retrieving

one of the packet rules from the first memory region and comparing packet data from a received packet, at the offset specified in the retrieved packet rule, to the data pattern specified in the retrieved packet rule, and, when the comparison evaluates true, incrementing a counter, at the counter offset specified in the retrieved packet rule, within a second memory region in the addressable memory space. The method further includes configuring the core processor to retrieve statistics from the counters in the second memory region.

According to another example embodiment, an article of manufacture includes computer-readable media containing instructions that, when executed by a network processor, cause that network processor to perform a method that includes dynamically accepting packet rule requests at a core processor and placing corresponding packet rules in a packet rule set area at a first memory region in an addressable memory space, at least one rule in the packet rule set specifying a packet offset, a data pattern, and a counter offset. The method further includes sequencing through the packet rule set with a set of packet processing engines, retrieving one of the packet rules from the first memory region and comparing packet data from a received packet, at the offset specified in the retrieved packet rule, to the data pattern specified in the retrieved packet rule, and, when the comparison evaluates true, incrementing a counter, at the counter offset specified in the retrieved packet rule, within a second memory region in the addressable memory space. The method further includes the core processor retrieving statistics from the counters in the second memory region for distribution outside of the network processor.

According to another example embodiment, an article of manufacture includes computer-readable media containing instructions that, when executed by a network processor, cause that network processor to perform a method that includes a core processor writing, to a shared memory accessible by the packet processing engines, a dynamic packet rule set, each rule specifying a packet offset, a data pattern, and an action code. The method further includes, on at least one packet processing engine, while processing a packet, loading a first packet rule from the packet rule set, comparing packet data at the packet offset specified in the first packet rule to the data pattern specified in the first packet rule, and, when the comparing step indicates a match, performing the action indicated by the action code specified in the first packet rule.